Planar Microwave and Millimeter-Wave Lumped Elements and Coupled-Line Filters Using Micro-Machining Techniques

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Abstract—**Planar microwave and millimeter-wave inductors and capacitors have been fabricated on high-resistivity silicon substrates using micro-machining techniques. The inductors and capacitors are suspended on a thin dielectric membrane to reduce the parasitic capacitance to ground. The resonant frequencies of a 1.2 nH and a 1.7-nH inductor have been increased from 22 GHz and 17 GHz to around 70 GHz and 50 GHz, respectively. We also report on the design and measurement of a new class of stripline filters suspended on a thin dielectric membrane. Interdigitated filters with 43% and 5% bandwidth have been fabricated and exhibit a port-to-port 0.7 dB and 2.0 dB loss, respectively, at 14–15 GHz. The micro-machining fabrication technique can be used with Silicon and GaAs substrates in microstrip or coplanar-waveguide configurations to result in planar low-loss lumped elements and filters suitable for monolithic integration or surface mount devices up to 100 GHz.**

I. Introduction

PLANAR lumped inductors and capacitors are used in microwave active and passive integrated circuits as matching elements, bias chokes and filter components. For frequencies below 12 GHz, these lumped elements are smaller than their transmission line equivalent circuits, and exhibit low-loss and wide bandwidth [1], [2]. Recently, planar inductors have been used at 26–40 GHz and their equivalent model has been calculated using a full-wave electromagnetic solution [3]. Still, the elements show a large capacitive components due to the parasitic capacitance between the elements and the ground plane. For planar inductors this results in a resonant frequency between 16 and 30 GHz. The planar interdigitated capacitors also suffer from a large parasitic capacitance to ground which affects their performance as true lumped element series capacitors [4].

We have solved the problem associated with the parasitic capacitance in planar inductors and capacitors by integrating them on a small dielectric membrane (Fig. 1). The thin dielectric membrane is defined underneath the lumped element and does not affect the propagation properties of the microstrip line or coplanar waveguide. The membrane is mechanically stable and is compatible with MMIC fabrication techniques (see Section II). The membrane is 1.2–1.4 μm thick and is very small compared to a wavelength at microwave and millimeter-wave frequencies. The membrane technology has been used before to build high performance millimeter-wave receivers [5], power meters [6], and recently, the dispersionless micro-shield transmission line [7], [8]. Also large suspended inductors on Silicon were fabricated by Chang *et al.* [9] in an 800 MHz RF amplifier. The planar inductors and capacitors are suspended in free-space and the quasistatic parasitic capacitance to ground is reduced by a factor of ϵ_r ($\epsilon_r = 11.7$ for high resistivity silicon). Also the quasistatic capacitance between the lines is reduced by a factor of $(1+\epsilon_r)/2$ since half the electric fields are in air and half the fields are in the dielectric [10]. This reduction in the parasitic capacitance increases the resonant frequency of the inductor without changing the inductance value and the associated series resistance. This results in planar inductors that can be used up to 60 GHz and higher and still have exactly the same geometries as their counterparts on Silicon or GaAs substrates.

We have also applied the micro-machining technique to planar interdigitated filters in a stripline circuit. This topology has been successfully used in low-loss wide-band and narrow-band filters at low microwave frequencies [11], [12]. The advantage of interdigitated filters is that they are physically very small and exhibit low insertion loss and a very sharp roll-off response. However, for designs at X-band frequencies and above, the gap between the coupled lines (fingers) and the height of the cavity become too small thus making the filter unrealizable. We have solved this problem by fabricating the interdigitated filter on a thin dielectric membrane (Fig. 2). The membrane approach also eliminates the dielectric loss which can be significant at millimeter-wave frequencies. The interdigitated filter is placed in a small cavity that is micro-machined in silicon to eliminate any radiation loss. The bottom part of the micro-machined cavity directly results from the etching of the silicon wafer. The top part of the micro-machined cavity is fabricated individually and placed on top of the planar filter using silver epoxy. The height of the top and bottom cavity, which is important to the filter design, is given by the thickness of the silicon wafers. An interdigitated filter can be easily fabricated at 60–90 GHz with a 100-μm-thick silicon (or GaAs) wafer.

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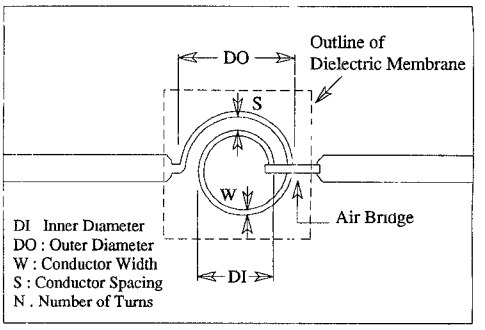
II. Fabrication

A three-layer structure of $SiO_2/Si_3N_4/SiO_2$ is deposited on a high-resisitivity silicon substrate using thermal oxidation and high-temperature chemical vapor deposition [6]. The layer must be in tension resulting in flat and rigid membranes once the silicon substrate is etched underneath the membrane. A thermal SiO_2 layer with a thickness of 5000 Å is first grown at a temperature of 1100°C. The wafer is then placed in a LPCVD (Low Pressure Chemical Vapor Deposition) furnace. A 3000 Å Si_3N_4 layer is deposited at 820°C. The gas flow rate are NH_3: 160 sccm and DCS: 40 sccm. Next a 4000 Å SiO_2 layer was deposited using the LPCVD furnace at 920°C. The gas flow rate are N_2: 290 sccm, N_2O: 120 sccm and DCS: 60 sccm. It is important to note that a membrane layer can also be fabricated using GaAs or InP substrates for active microwave circuit applications. In this case, the membrane layer is deposited using plasma enhanced chemical vapor deposition (PECVD). The deposition parameters of the PECVD layer must also be adjusted so as to result in a tensile layer (in contrast to a layer under compressive stress) [13]. After the layer is deposited on the silicon or GaAs substrate, the planar element is defined on the top side of the substrate using standard lithography, gold evaporation and electroplating. Next, an opening is defined in the membrane on the back side of the wafer just underneath the planar lumped element or filter, and the silicon or GaAs substrate is etched until the transparent dielectric membrane appears (Fig. 3). The etchant used with silicon wafers is KOH or EDP [14]. The etchant used with GaAs wafers is an $H_2SO_4/H_2O_2/H_2O$ based solution or dry etching in an RIE machine [13]. In GaAs substrates, this procedure is totally compatible with via-hole formation which is used to contact the source-terminals in 3-terminal devices to the RF ground-plane at the back-side of the substrate, or to eliminate substrate modes in grounded-CPW designs.

In the case of the suspended stripline interdigitated filters, additional processing is needed to complete the filter. A row of via holes is etched around the membrane cavity and electroplated with gold to connect the RF short (ground-plane) next to the membrane to the bottom ground plane (see Fig. 2). The via-holes also eliminate any loss to substrate modes that are excited in the electrically thick Silicon or GaAs substrate. Next, a silicon wafer is etched and electroplated to form the top cavity and placed on top of the membrane. The thickness of the top silicon wafer and the membrane wafer are part of the design parameters of the interdigitated filters (see Section V).

III. Microwave Measurements: Inductors

Two planar microstrip inductors were fabricated on a 355-μm-thick high-resistivity silicon substrate. Identical inductors using the same masks were also fabricated on a 1.2-μm-thick dielectric membrane using the micro-machining technique outline previously. The membrane edge is aligned with the physical edge of the inductor as shown in Fig. 1. The microstrip line is 1 μm-thick electroplated gold and the air-bridge dimensions are 250 μm $\times$ 40 μm and is 2 μm high using electroplated gold. Two completed inductors are shown in Fig. 4. The microstrip inductor dimensions are outlined in Table I and are designed to yield an inductance value of 1.09 nH and 1.69 nH by using the following equation from [10]:



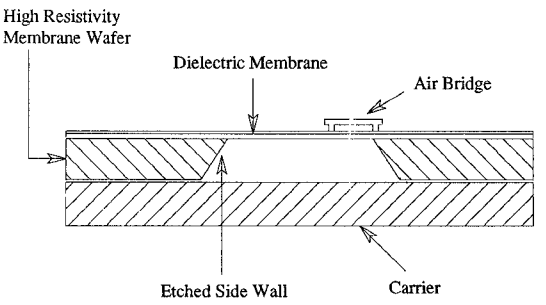


Fig. 1. Layout of the planar inductor and the membrane outline. The membrane is defined only underneath the planar lumped elements.

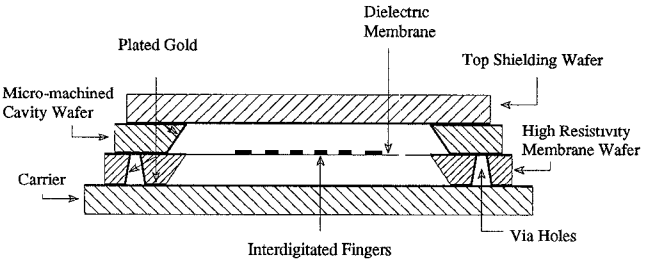


Fig. 2. Cross-sectional view of the suspended interdigitated filter.

$$L_s(\text{nH}) = 0.01AN^2\pi[\ln(8A/C) + (1/24)(C/A)^2\ln(8A/C + 3.583) - 1/2] \quad (1)$$

where $A = (DO + DI)/4$, $C = (DO - DI)/2$ (see Fig. 1), A and C are given in "mils" (1 mil = 25.4 μm) and N is the number of turns.

The TRL calibration routine is used to measure the loss of the 50 Ω microstrip line on a high resistivity silicon substrate (2000 Ωcm) which is attached to the lumped inductor. The microstrip line is 1 mm long on each side of the inductor and exhibits a loss of 0.2 dB/mm from 3–20 GHz. This implies that the loss of the microstrip line is dominated by dielectric loss in the substrate. The microstrip line loss is modeled as a matched attenuator (R_1, R_2, R_3). The reference plane for the inductor measurements is defined at the outer limit of the inductor geometries or simultaneously at the edge of the membrane (Fig. 1).

The measured and modeled 3–20 GHz Reactance (X) of the inductors on a thick silicon substrate (L_{1S}, L_{2S}) and

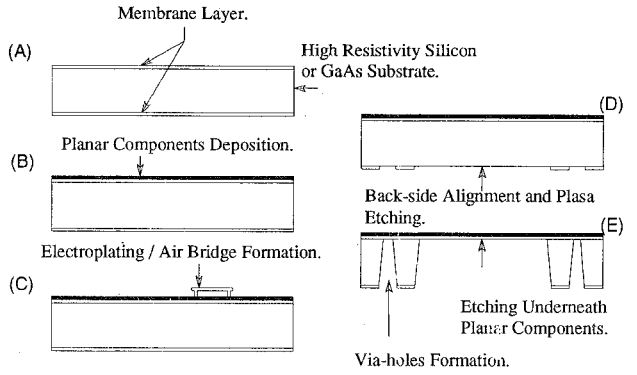


Fig. 3. Fabrication procedure of the micro-machined planar elements. This is compatible with GaAs and InP via-hole process technology.

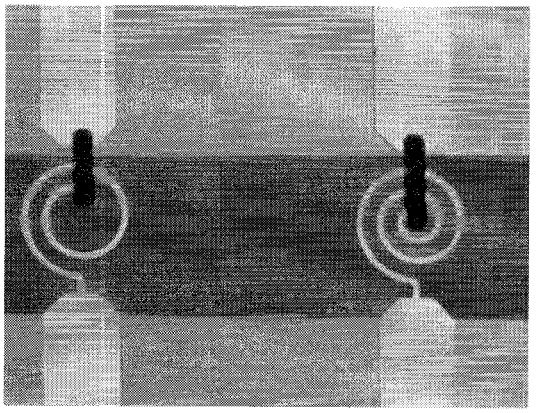
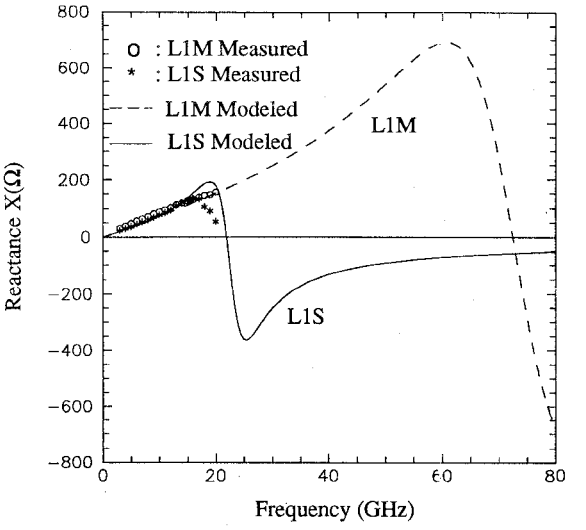


Fig. 4. Micro-machined inductors L_{1M} (left) and L_{2M} (right) on a small dielectric membrane and their equivalent model. A 0.2 dB attenuator is placed at each end to model the loss in the 50 Ω microstrip line on the high-resistivity Silicon dielectric substrate.

TABLE I
PHYSICAL DIMENSIONS AND THE CORRESPONDING CALCULATED INDUCTANCE VALUES FOR THE SPIRAL INDUCTORS. ALL UNITS ARE IN μm (SEE FIG. 1)

Components	DI	DO	W	S	N	L_s(nH)
L_{1S}, L_{1M}	254	406.4	25.4	50.8	1.5	1.09
L_{2S}, L_{2M}	101.6	406.4	25.4	50.8	2.5	1.69

the inductors on a thin dielectric membrane (L_{1M}, L_{2M}) is shown in Fig. 5. The equivalent model of the silicon inductors (L_{1S}, L_{2S}) is used to fit the measured S-parameters (not shown) using the EESof-Touchstone optimization routine. The equivalent values of L_s, R_s, C_p, C_s are summarized in Table II. It is seen that the equivalent inductance agrees quite well with (1) and the resonant frequency is 22 GHz and 17 GHz for a 1.2 nH and a 1.7 nH planar microstrip inductor, respectively. The same model is used for the membrane planar inductors, with C_p reduced by a factor of ϵ_r ($\epsilon_r = 11.7$) and C_s reduced by a factor of approximately (1+ ϵ_r)/2 (Table II). The inductance L_s and the resistance R_s are not changed since



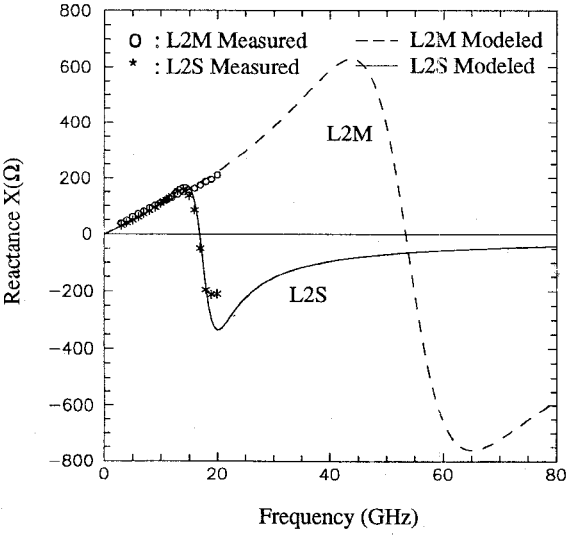


Fig. 5. Measured and modeled reactance (X) of L_1 and L_2 (M stands for membrane supported and S for substrate supported).

the membrane and silicon inductors have identical geometries. It is seen that the measured Reactance (X) of the membrane inductors (L_{1M}, L_{2M}) agree well with the simple equivalent model (3–20 GHz). The resonant frequency of the membrane inductors is pushed to around 70 and 50 GHz for a 1.2 and 1.7 nH inductor, respectively. The parasitic capacitances are very low for the micro-machined inductors (C_p, C_s =2–4 fF) and the membrane inductors can be used as "true" inductors up to 40–60 GHz. The model takes into account only the quasistatic capacitance of the lumped inductor and neglects the transmission- line effects of the pyramidal cavity underneath the lumped inductor. At mm-wave frequencies, the membrane inductors may result in lower resonant frequencies as predicted above due to non quasistatic (high-order modes) effects.

The micro-machined inductors behave exactly the same way as the standard planar microstrip inductors at microwave frequencies. Therefore, it is expected that the micro-machined inductor will exhibit a similar Q at microwave frequencies. A small LC series filter composed of a membrane inductor of value 0.9 nH (with a series resistance, $R_s \simeq$ 1.2–1.3 Ω) and

TABLE II
MODELED VALUES OF R_s, L_s, C_s, C_p FOR SPIRAL INDUCTORS ON SILICON AND MEMBRANE SUBSTRATE (SEE FIG. 4)

Components	$R_s(\Omega)$	L_s(nH)	C_s(fF)	C_p(fF)
L_{1S}	3	1.2	10	33
L_{1M}	3	1.2	**2**	**2.5**
L_{2S}	5	1.7	6	45
L_{2M}	5	1.7	**1.2**	**4**

a chip capacitor of value 1.2 pF was fabricated. The chip capacitor is a surface mount MIS type capacitor (Metelics MBIC-1002) and has a very high Q up to 12 GHz, and its effect on the measured Q is neglected at 4.3 GHz. The measured S_{11} of the series LC combination demonstrates a quality factor of $Q = 20$ at 4.3 GHz for the membrane inductor and is closed to the expected value from the equation $Q = \omega_0 L/R_s$ (Fig. 6). The measurements include the effect of the bond wires used to connect the silicon substrate to the coaxial connectors ($L_{\text{bw}} \simeq 0.1$ nH). The associated Q of membrane inductors is expected to increase as $\sqrt{f}$ with frequency (because the series resistance increases as $\sqrt{f}$ [10]) to yield a Q of 50–60 at 30–40 GHz.

IV. MICROWAVE MEASUREMENTS: CAPACITORS

A similar fabrication technique was applied to planar interdigitated capacitors. In this case, the planar capacitors do not suffer from a low resonant frequency but from a relatively large shunt parasitic capacitance to ground (C_p). During modeling the parasitic capacitance to ground is generally included with the interdigitated series capacitance (C_s). However, it is advantageous to eliminate this parasitic capacitance to result in better millimeter-wave filters, phase shifters and matching networks. The micro-machined membrane approach reduces the parasitic capacitance by a factor of ϵ_r. However, in this case, it also reduces the interdigitated series capacitance by a factor of $(1+\epsilon_r)/2$.

An eight finger and a four finger interdigitated capacitors were fabricated on a high resistivity silicon substrate and on a membrane. The capacitor finger is 355 μm long and is 25 μm wide. The gap between the fingers is also 25 μm wide. The measured S_{11} from 7 to 20 GHz for the capacitors are shown in Fig. 7. It is seen that the membrane interdigitated capacitor (of value around 110 fF for the eight finger capacitor and 55 fF for the four finger capacitor) follows the 1-jx line on the Smith chart as expected from a capacitor in series with a 50 Ω load. The interdigitated capacitor on the silicon dielectric shows a large shunt capacitance effect due to the parasitic capacitance to ground. The measured S_{11} of the capacitors on the silicon substrate agree very well with published results of similar capacitors on GaAs substrates [4]. Compared with dielectric supported capacitors, it is seen that the micro-machined membrane capacitors demonstrates a much better performance at microwave frequencies. The quality factor of the membrane capacitors was not measured at microwave frequencies but is expected to be larger than the corresponding capacitors on the silicon substrate due to the absence of the dielectric losses.

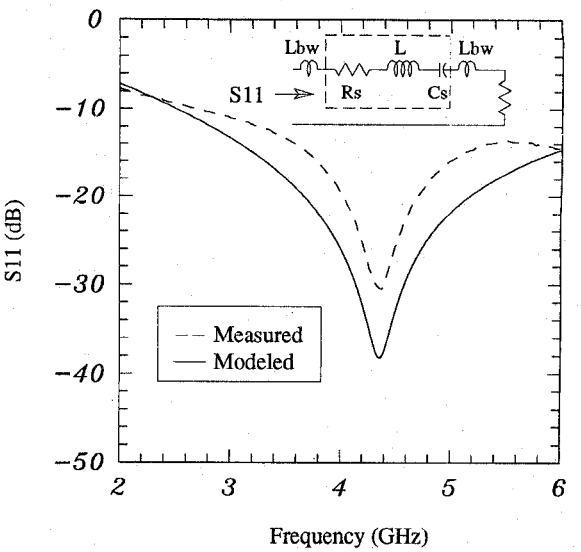


Fig. 6. Measured and modeled S_{11} of a series LC filter with a micro-machined membrane inductor. The measured quality factor (Q) is equal to 20 at 4.3 GHz.

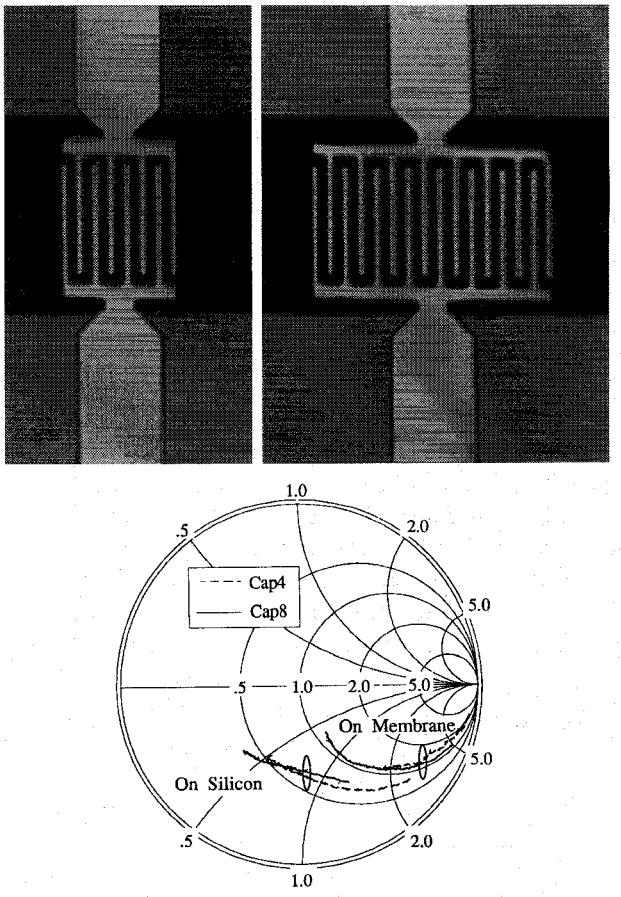
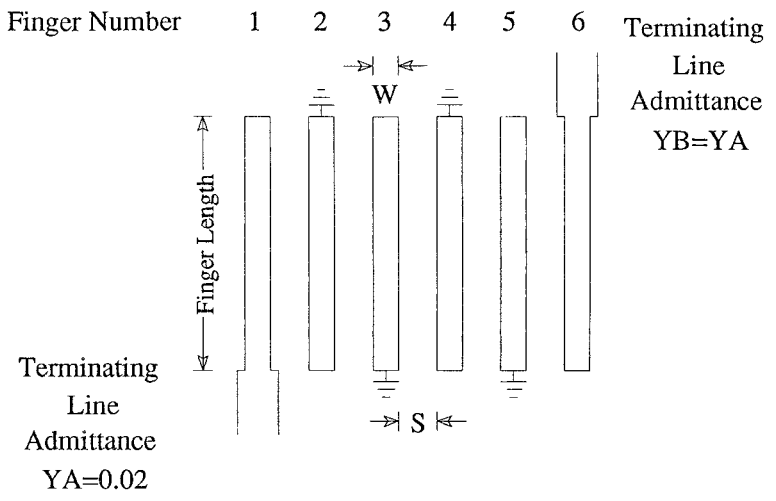


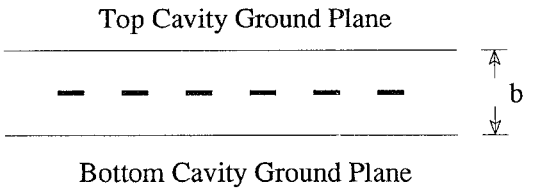
Fig. 7. Micro-machined capacitor Cap4M (top left) and Cap8M (top right) on a small dielectric membrane and the measured 7–20 GHz S_{11} of the two interdigitated capacitors.

V. INTERDIGITATED SUSPENDED-FILTER DESIGN

The interdigitated suspended filter design follows the bandpass filter design which is elegantly presented by Matthaei in [11], [12], [15], [16]. Briefly, a low-pass filter prototype is



(a)



(b)

K	$C_{k,k+1}/\epsilon$	$s_{k,k+1}(\mu m)$	$C_{fe_{k,k+1}}/\epsilon$	$C_{fo_{k,k+1}}/\epsilon$	K	C_k/ϵ	$w_k(\mu m)$
1, 5	0.885	115	0.142	1.027	1, 6	1.694	122
2, 4	0.762	141	0.168	0.930	2, 5	2.405	317
3	0.729	149	0.176	0.905	3, 4	2.399	304
$\omega = 0.4$				b = 710μm			
$\epsilon_r = 1.0$				finger length = 4.75 mm			

(c)

Fig. 8. (a) A wide-band 6-section interdigitated filter. Notice, it is open-circuited design at the input and output fingers. (b) Cross-sectional view of this filter. (c) Tabulation of quantities for a 40% 6-section 0.05-dB equal ripple filter design.

used to determine the band-pass filter characteristics and the low-pass filter is modified with appropriate inverters to result in a totally capacitive filter. Each section of the capacitive filter is then modeled by an equivalent interdigitated coupled line and the values are matched at the design frequency f_0. This results in the total self capacitance (C_k) and the mutual capacitance $(C_{k,k+1})$ of the equivalent interdigitated coupled line stage [16]. The even $(C_{f_{e_{k,k+1}}})$ and odd-mode $(C_{f_{0\,k,k+1}})$ fringing capacitances of suspended coupled lines are given by Cohn [17]:

$$\frac{C_{f_{e_{k,k+1}}}\left(\frac{s_{k,k+1}}{b}\right)}{\epsilon} = \frac{s_{k,k+1}}{b} - \frac{2}{\pi}\ln\left(\cosh\frac{\pi s_{k,k+1}}{2b}\right) \quad (2)$$

$$\frac{C_{f_{0_{k,k+1}}}\left(\frac{s_{k,k+1}}{b}\right)}{\epsilon} = \frac{s_{k,k+1}}{b} - \frac{2}{\pi}\ln\left(\sinh\frac{\pi s_{k,k+1}}{2b}\right) \quad (3)$$

where b is the distance between the two parallel ground planes and $s_{k,k+1}$ is the distance between two interdigitated finger $k, k+1$ (see Fig. 8b).

The mutual capacitance $(C_{k,k+1})$ is the difference between the odd $(C_{f_{0_{k,k+1}}})$ and even-mode $(C_{f_{e_{k,k+1}}})$ fringing capacitances. Therefore, the mutual capacitance, $C_{k,k+1}$, can also be written as:

$$\frac{C_{k,k+1}}{\epsilon} = \frac{C_{f_{0_{k,k+1}}}}{\epsilon} - \frac{C_{f_{e_{k,k+1}}}}{\epsilon}. \quad (4)$$

The spacing $s_{k,k+1}$ between two fingers can then be solved by substituting (2) and (3) into (4) and is given by

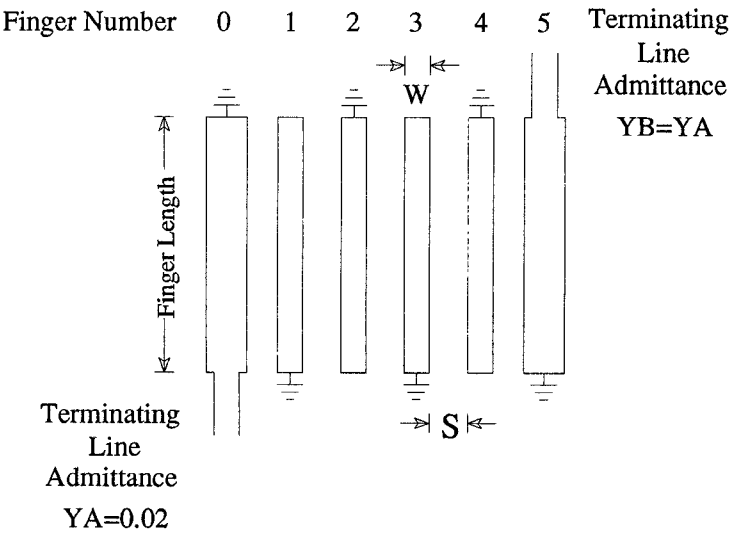
$$s_{k,k+1} = \frac{2b}{\pi}\tanh^{-1}\left[\exp\left(\frac{-\pi C_{k,k+1}}{2\epsilon}\right)\right]. \quad (5)$$

After the spacing $s_{k,k+1}$ has been calculated, the even-mode fringing capacitance $(C_{f_{e_{k,k+1}}})$ between the two adjacent fingers can be obtained from (2) (or the odd mode fringing capacitance $(C_{f_{0_{k,k+1}}})$ from (3)). The line width of each finger (w_k) can be calculated knowing C_k (the self capacitance of finger k) and using the equation given by Getsinger [18].

$$w_k = \frac{b}{2}\left[\frac{1}{2}\frac{C_k}{\epsilon} - \frac{C_{f_{e_{k-1,k}}}}{\epsilon} - \frac{C_{f_{e_{k,k+1}}}}{\epsilon}\right]. \quad (6)$$

If the w_k/b ratio in (6) is less than 0.35, the width of the stripline should be corrected using the approximate formula:

$$w_k' = \frac{0.07b + w_k}{1.20} \quad (7)$$



(a)

K	$C_{k,k+1}/\epsilon$	$s_{k,k+1}(\mu m)$	$C_{fe_{k,k+1}}/\epsilon$	$C_{fo_{k,k+1}}/\epsilon$	K	C_k/ϵ	$w_k(\mu m)$
0, 4	1.376	52	0.069	1.445	0, 5	6.159	923
1, 3	0.205	416	0.347	0.552	1, 4	3.689	508
2	0.154	479	0.369	0.523	2, 3	4.664	575
$\omega = 0.05$				b = 710μm			
$\epsilon_r = 1.0$				finger length = 4.32 mm			

(b)

Fig. 9. (a) A narrow-band 4-section interdigitated filter. Notice that it is short-circuited at the input and output fingers. (b) Tabulation of quantities for a 5% four-section 0.025-dB equal ripple filter design.

where w_k is the uncorrected stripline width and w'_k is the corrected width [18].

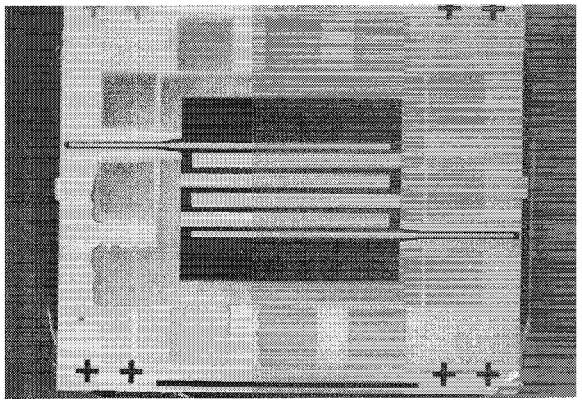
The calculated coupling capacitances and dimensions for a wide-band (40%) 6-stage 0.05 dB equal ripple filter and a narrow-band (5%) 4-stage 0.025 dB equal ripple filter are shown in Figs. 8 and 9. The filters are designed for a center frequency of 15 GHz. The cavity height is chosen to be 710 μm and is constructed using two 355 μm standard silicon wafers. The metal thickness is 3 μm electroplated gold for the wide-band design and 5 μm for the narrow-band design. The top cavity is electroplated gold to about 3 μm thick in both filter designs. The fabricated filters are shown in Fig. 10. A row of via holes with a spacing of 2 mm ($\simeq\lambda_d/3$) is etched around the membrane cavity to connect the RF short (ground-plane) next to the membrane to the bottom ground plane (see Fig. 2). The via holes are filled with silver epoxy but can be directly electroplated with gold in monolithic fabrication techniques.

VI. Interdigitated Suspended-Filter Measurements

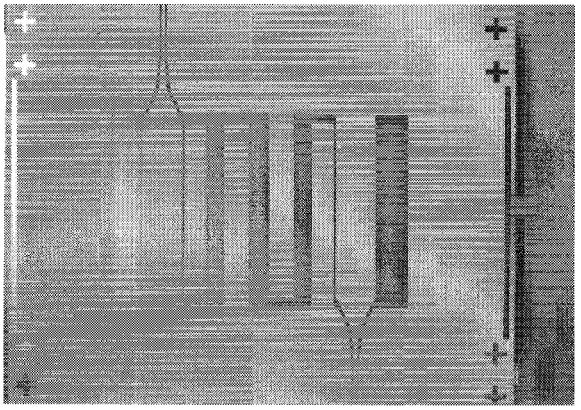
A. Wide-Band Interdigitated Filter (40%)

The wide-band planar interdigitated filter is fed by a 50 Ω grounded-CPW transmission line and is compatible with a 150 μm-pitch CPW-based Cascade probe. The filter can also be designed to have a microstrip input feed line. The measurement system is calibrated using a SOLT (Short-Open-Load-Thru) routine which sets the reference plane at the probe tips. Two wide-band planar filters were measured yielding nearly identical results ($\pm$0.05 dB in insertion loss). Each feed line is 2.6 mm long and has a measured insertion loss of around 0.2 dB at Ku band. Each finger is 4.75 mm long and the membrane dimensions are 5 mm long and 4.2 mm wide. The fingers are not 5 mm long ($\lambda_0/4$) since they do take into account the extra fringing capacitance at their tip [10].

The measured port-to-port filter response is shown in Fig. 11. It is seen that the filter has a 10.3–16.8 GHz 3-dB pass-band with a port-to-port insertion loss of 0.7 dB at the center frequency (including the loss of the two feed lines). The performance of this filter is competitive with the best stripline designs available in the literature [19], [20]. Since this filter was designed to have an equal ripple response, the definition of pass-band is smaller than the usual 3-dB bandwidth definition. The equal ripple bandwidth of this filter is 43% which is very closed to the designed 40% bandwidth. The center frequency shifted to 13.7 GHz. We feel that this is due to several factors such as the exact placement of the via holes surrounding the membrane (5.4 mm) and the dimensions of the top cavity (5.4 mm-square). This was done to aid in the alignment process and in hindsight was larger than necessary. The center frequency shifted by 10% down due to these processes. In the future, tighter control on the dimensions should be maintained in the micro-machining techniques, or an FDTD analysis should be done to predict the exact center frequency. The low-frequency roll-off response is very sharp with a 60 dB rejection at 5.8 GHz. The high frequency roll-off is also sharp with a 55 dB rejection at 2 f_0. The shape of the measured pass-band response is slightly unsymmetric. This is due to the nature of



(a)



(b)

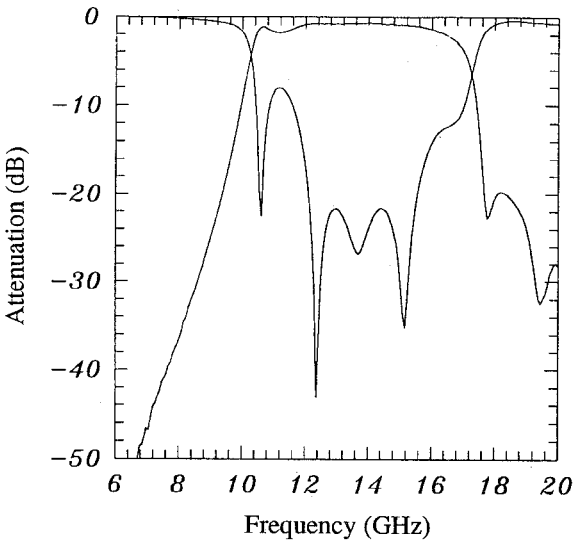
Fig. 10. Picture of the fabricated devices (a) for the 40% filter and (b) of the 5% filter. The dark area in the center of (a) and the white area in the center of (b) is the membrane and the squares around the membrane correspond to via holes. The input/output transmission line is grounded CPW.

the unsymmetric coupled- line filter design since each coupled line has a different width. As can be seen, the filter is repetitive at 3 f_0 which is around 41 GHz and beyond our measurement setup.

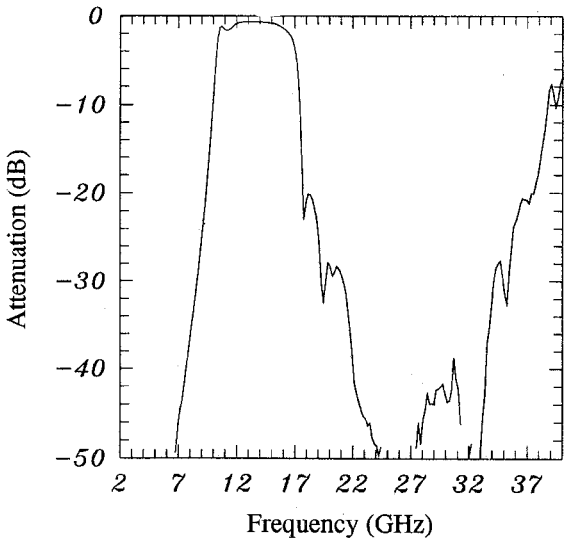
The same filter was measured without the top shielding wafer. The filter preserves the band-pass characteristics but the bandwidth increases from 6.5 GHz (43%) to 9.1 GHz (66%). The filter operates in stripline mode with the top-shielding wafer, or microstrip mode without it. As a result, the coupling capacitance between a pair of coupled lines becomes stronger, and this causes the increase in bandwidth. For both filters, with and without a top shielding wafer, the propagation media is air only, and there is no other dielectric material involved. Therefore, the filters propagate a dispersionless TEM mode. This can be seen from the measurements of group delay (Fig. 12) which show a constant group delay over the entire operating bandwidth of both filters.

B. Narrow-Band Interdigitated Filter (5%)

A narrow-band filter was fabricated and measured using the same approach outlined above. Two narrow-band planar filters were measured also yielding nearly identical results (± 0.1 dB in insertion loss). In this case, the finger length is 4.3 mm and the membrane dimensions are about 4.5 × 7 mm. The top cavity dimensions and the exact placement of the



(a)



(b)

Fig. 11. Measured response of the wide-band 40% interdigitated filter (a) S_{11} and S_{21} from 6–20 GHz and (b) S_{21} from 2–40 GHz.

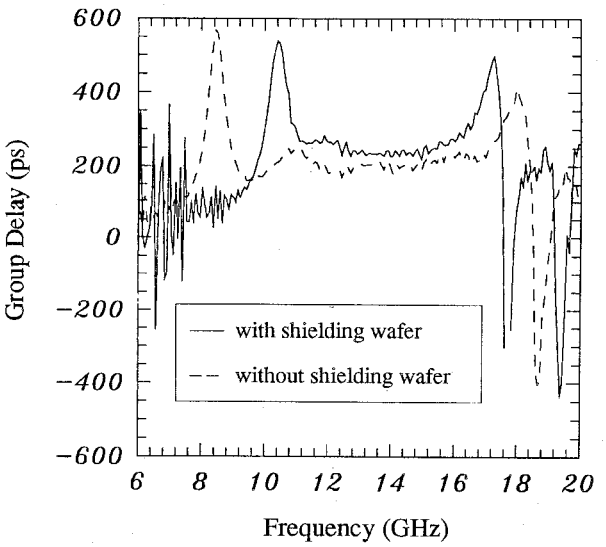


Fig. 12. Measured group delay for the wide-band 40% interdigitated filter.

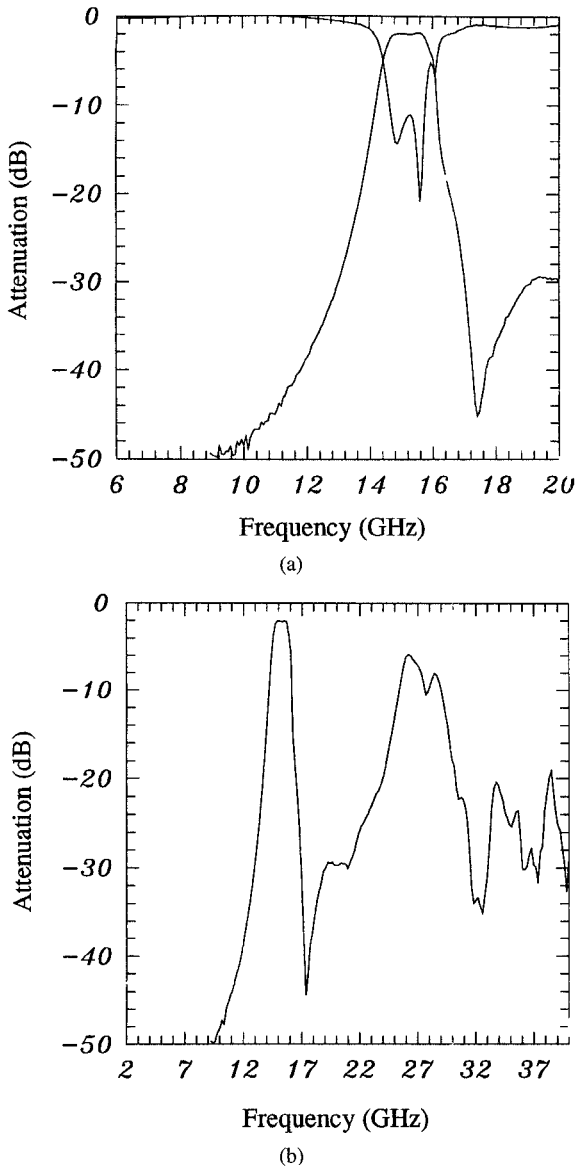


Fig. 13. Measured response of the narrow-band 5% interdigitated filter (a) S_{11} and S_{21} from 6 to 20 GHz and (b) S_{21} from 2 to 40 GHz.

via-holes around the membrane are again about 10% larger than the membrane dimensions. However, the finger length and the membrane length (in the resonant dimension) have been reduced by 10% to counteract this effect.

The measured port-to-port filter response is shown in Fig. 13. It is seen that the filter has a 14.8–15.6 GHz equal-ripple pass-band with a port-to-port insertion loss of 2.0 dB at the center frequency of 15.2 GHz (including the loss of the two feed lines, 0.4 dB, and the 0.5 dB return loss from S_{11} data). The 1.1 dB residual loss can be traced fully to the Ohmic loss in the narrow-band interdigitated design [21]. The measured equal-ripple bandwidth is 5.5%. The filter shows a very sharp skirt with a 40 dB rejection at 12 and 17 GHz. It is interesting to note that this filter shows a near-repetitive performance at 2 f_0 due to parasitic coupling capacitance between the tip of the fingers and the surrounding ground plane. This capacitance dominates over the weak coupling capacitance between the interdigitated fingers at 2 f_0 and renders the filter a capacitively loaded comb-line filter [16]. This can be minimized by placing the tip of the fingers far away from the membrane edge.

VII. Conclusion

We have introduced a new micro-machining technique that allows us to build high quality lumped elements and interdigitated filters for the microwave and millimeter-wave band. The membrane inductors and capacitors built using this technique have shown a much better performance than their Silicon/GaAs counterparts. The interdigitated filters have also shown excellent performance at 13–15 GHz and the designs can be extended to millimeter-wave frequencies. The micro-machining technique is compatible with all types of transmission lines, such as the microstrip, the coplanar-waveguide and the stripline guide media. Furthermore, it can be used with standard MMIC fabrication or for high-quality surface-mount elements and sub-systems. The micro-machining technique will benefit greatly from the upcoming FDTD analysis methods to predict the effect of nonvertical cavity walls, nonvertical via-holes and the transition between the high dielectric constant substrate and the membrane supported element.

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References

[1] R. A. Pucel, "Design considerations for monolithic microwave circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, no. 6, pp. 513–534, June 1981.

[2] G. D. Alley, "Interdigital capacitors and their application to lumped-element microwave integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-18, pp. 1028–1033, Dec. 1970.

[3] M. Abdo-Tuko, M. Naghed and I. Wolff, "Novel 18/36 GHz (M)MIC GaAs FET frequency doublers in CPW-techniques under the consideration of the effects of coplanar discontinuities," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-41, no. 8, pp. 1307–1315, Aug. 1993.

[4] R. Esfandiari *et al.*, "Design of interdigitated capacitors and their application to gallium arsenide monolithic filters," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-31, no. 1, pp. 57–64, Jan. 1983.

[5] W. Y. Ali-Ahmad, W. L. Bishop, T. W. Crowe and G. M. Rebeiz, "An 86–106 GHz quasiintegrated low noise Schottky receiver," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-41, no. 4, pp. 558–564, Apr. 1993.

[6] C. C. Ling and G. M. Rebeiz, "A wide-band monolithic quasioptical power meter for millimeter- and submillimeter-wave applications," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-39, no. 8, pp. 1257–1261, Aug. 1991.

[7] S. V. Robertson, L. P. Katehi and G. M. Rebeiz "W-band microshield low-pass filter," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1993, pp. 625–628.

[8] L. P. Katehi *et al.*, "Micromachined circuits for millimeter- and submillimeter-wave applications," *Antennas and Propagation Mag.*, pp. 9–17, Oct. 1993.

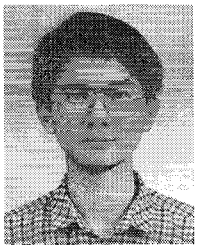
[9] J. Y. Chang, A. A. Abidi, and M. Gaitan "Large suspended inductors on silicon and their use in a 2-μm CMOS RF amplifier," *IEEE Electron Dev. Lett.*, vol. 14, no. 5, pp. 246–248, May 1993.

[10] K. C. Gupta, R. Garg, and R. Chadha, *Computer-Aided Design of Microwave Circuits.* Norwood, MA: Artech House, 1981.

[11] G. L. Matthaei, "Interdigital band-pass filters," *IRE Trans. Microwave Theory Tech.*, vol. PGMTT-10, pp. 479–491, Nov. 1962.

[12] G. L. Matthaei and G. L. Hey-Shipton "Novel staggered resonator array superconducting 2.3 GHz bandpass filter," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-41, no. 12, pp. 2345–2352, Dec. 1993.

[13] R. E. Williams, *Modern GaAs Processing Methods.* Norwood, MA: Artech House, 1992.
[14] K. E. Petersen, "Silicon as a mechanical material," *Proc. IEEE.*, vol. 70, no. 5, pp. 420–457, May 1982.
[15] G. L. Matthaei, "Design of wide-band (and narrow-band) band-pass microwave filters on the insertion loss basis," *IRE Trans. Microwave Theory Tech.*, vol. PGMTT-8, pp. 580–593, Nov. 1960.
[16] G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures.* Norwood, MA: Artech House, 1980, ch. 10, pp. 614–650.
[17] S. B. Cohn, "Shielded coupled-strip transmission line," *IRE Trans. Microwave Theory Tech.*, vol. MTT-3, pp. 29–38, Oct. 1955.
[18] W. J. Getsinger, "Coupled rectangular bars between parallel plates," *IRE Trans. Microwave Theory Tech.*, vol. PGMTT-10, pp. 65–72, Jan. 1962.
[19] G. E. Johnson and M. D. Medley, "A novel approach for integrating high-Q band-pass filters into microwave integrated circuit assemblies," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1993, pp. 1309–1311.
[20] M. Miyazaki, H. Asao and O. Ishida, "A broadband dielectric diplexer using a snaked strip-line," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1991, pp. 551–554.
[21] "Parfil," version 2.3, WaveCon, Escondido, CA.



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